wherein said second surface roughness value is sufficiently small to provide a substantially planar surface on said substrate whereon a plurality of structures may be formed to define a plurality of transistors.

28. (New) The method of claim 27, wherein said cleaved surface is free of any transistor-related structure. --

REMARKS

Claims 9-28 are pending. Claims 1-8 have been canceled. New claims 9-28 are added. No new matter has been added. Support for claim 19, i.e., the phrase "wherein said cleaved surface is substantially planar," is provided at least on page 4, lines 9-14 and by Fig. 5. Similarly, support for claim 27 is provided at least on page 4, lines 9-14 and by Fig. 5.

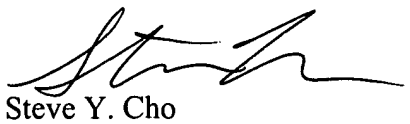
Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

On page 1, the following paragraph has been added after the title of the invention:

-- This is a continuation of U.S. Patent No. 6,287,941, which claims priority to U.S. Provisional Patent Application No. 60/130,423, filed on April 21, 1999, which are incorporated by reference herein for all purposes. --

IN THE CLAIMS:

The claims have been amended as follows:

Claims 1-8 have been canceled.

The following new claims have been added.

-- 9. (New) A method for manufacturing of substrates including treatment a film of material, said method comprising:

providing a substrate comprising a surface, said surface having an initial surface roughness value;

increasing a temperature of an environment associated with said surface to is about 1,000° Celsius or greater; and

exposing said cleaved surface to a hydrogen bearing environment at least when said temperature of said environment is about 1000° Celsius or greater to reduce said initial surface roughness value by at least about thirty percent, said hydrogen bearing environment including a halogen gas and a hydrogen gas.

10. (New) The method of claim 9, wherein said halogen gas is HCl.

11. (New) The method of claim 10 wherein said initial surface roughness value is reduced by at least about fifty percent.

12. (New) The method of claim 11 wherein said HCl gas and said hydrogen gas is at a ratio of about 0.001 to 30.

13. (New) The method of claim 9, wherein said halogen gas interacts with said surface to reduce said surface roughness value.

14. (New) The method of claim 9 wherein said initial surface roughness value of said surface is reduced in a thermal processing chamber.

15. (New) The method of claim 9 wherein cleaved surface is provided by a controlled cleavage process.

16. (New) The method of claim 9 wherein said substrate is a silicon wafer.

17. (New) The method of claim 9, wherein said environment is said surface.

18. (New) The method of claim 9, wherein said environment is a process chamber wherein said substrate is provided.

19. (New) A method for manufacturing a substrate having a cleaved surface with a first surface roughness value, said method comprising:

increasing a temperature of an environment of said cleaved surface to about 1,000° Celsius or greater; and

exposing said cleaved surface to an etchant at least when said temperature of said environment is about 1000° Celsius or greater to reduce said first surface roughness value to a second surface roughness value, wherein said cleaved surface with said second surface roughness value is substantially planar.

20. (New) The method of claim 19, wherein said second surface roughness value is less than said first surface roughness value by about thirty percent or more.

21. (New) The method of claim 19, where said etchant contains hydrogen.

22. (New) The method of claim 19 wherein said etchant is HCl, and said cleaved surface is exposed to a hydrogen gas.

23. (New) The method of claim 19 wherein said substrate is processed to define a plurality of structures in order to form a plurality of transistors thereon.

24. (New) The method of claim 19, wherein said substrate is free of a transistor-related structure on said cleaved surface, said transistor-related structure being a structure that is provided on said cleaved surface to define one or more transistors on said substrate.

25. (New) The method of claim 19, wherein said substrate is a silicon substrate, said method further comprising:

exposing said cleaved surface to a silicon bearing gas to provide silicon atoms thereon while said cleaved surface is being etched by said etchant.

26. (New) The method of claim 19, wherein said cleaved surface has a particular level of hydrogen concentration, said method further comprising:

treating said cleaved surface to increase said hydrogen concentration level prior to increasing said temperature of said environment to about 1,000° Celsius or greater.

27. (New) A method for manufacturing a silicon substrate having a cleaved surface with a first surface roughness value, said method comprising:

increasing a temperature of said cleaved surface to 1,000° Celsius or greater;

exposing said cleaved surface to a hydrogen gas and an etchant at least when said environment of said cleaved surface is 1,000° Celsius or greater to reduce said first surface roughness value to a second surface roughness value; and

exposing said cleaved surface to a silicon bearing gas to provide silicon atoms thereon,

wherein said second surface roughness value is sufficiently small to provide a substantially planar surface on said substrate whereon a plurality of structures may be formed to define a plurality of transistors.

28. (New) The method of claim 27, wherein said cleaved surface is free of any transistor-related structure. --